

What is claimed is:

1. A semiconductor device comprising:

a first conductive layer formed of a surface of a substrate;

a second conductive layer which is formed close to
5 said first conductive layer and which is electrically isolated from said first conductive layer through an insulating layer,

wherein said first conductive layer is filled in a first through hole which is formed to pass through at least
10 a part of said insulating layer,

said second conductive layer is filled in a second through hole which is formed to pass through at least a part of said insulating layer,

a cross section of said first through is rectangular,
15 in which said first through hole has a wider surface which is confronted with said second through hole, and

a cross section of said second through is rectangular, in which said first through hole has a wider surface which is confronted with said second through hole,
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2. The semiconductor device according to claim 1, wherein a load capacitance is produced between said first conductive layer and said second conductive layer in a direction of thickness of said first and second conductive
25 layers.

3. The semiconductor device according to claim 1, wherein a top surface of said first conductive layer is coupled to a first metallic wiring, and said second conductive layer is couple to a second metallic wiring.

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4. The semiconductor device according to claim 3, wherein said first metallic wiring is connected with a first power source, and said second metallic wiring is connected with a second power source.

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5. The semiconductor device according to claim 3, wherein an interval between said first and second through holes is narrower than an interval between said first and second metallic wirings.

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